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3.2.1 Institution has created an ecosystem for innovations and has initiatives for creation and transfer of knowledge (patent filed, published, incubation center facilities in the HEI to be considered)

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List of Seminars/Workshops

A.Y.2022-23

S.No	Name of the workshop/ seminar/ conference	Number of Participants	Date
1	Research and Development on Low Power Techniques in VISI Design	32	22/11/2022
2	Entrepreneurship as a career option	38	12/11/2022
3	Research and Methadology on Thesis and paper writing	32	15/10/2022
4	Entrepreneurship Development Programme	33	20/08/2022

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List of Seminars/Workshops

A.Y.2021-22

S.No	Name of the workshop/ seminar/ conference	Number of Participants	Date
1	IPR With Trips Agreement involved In Trademarks	36	18/07/2022
2	Research trends in Natural Language Processing	32	16/03/2022
3	Competitive advantage	37	12/02/2022
4	Intellectual Property Rights With Trades	42	15/02/2022
5	Technology Based Entrepreneurship Development programme	42	13/12/2021
6	Entrepreneurship skills and Bussiness and Development	38	11/12/2021
7	Use & Misuse Of IPR	38	09/12/2021
8	Analytical Research Methadology of RP-HPLC	28	16/11/2021
9	Research Trends in Digital Signal Processing using FPGA	27	16/11/2021
10	Consumer Awareness	41	20/11/2021
11	Trademark And Circular Its Inter Disciplinary Relation With Copyrights	41	10/11/2021
12	Intellectual Property Rights On Patents	43	30/10/2021
13	Research and Development in Cloud computing	43	28/09/2021
14	Employment opprtuities	37	11/09/2021

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List of Seminars/Workshops

A.Y.2020-21

S.No	Name of the workshop/ seminar/ conference	Number of Participants	Date
1	Emerging Trends On Intellectual Property Rights	38	08/02/2021
2	Six sigma(green belt)	41	28/01/2021
3	Intellectual Property Rights Relevance And Importance In The Global Era	36	18/12/2020

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List of Seminars/Workshops

A.Y.2019-20

S.No	Name of the workshop/ seminar/ conference	Number of Participants	Date
1	Business Operator	47	24/02/2020
2	Clinical Research Methodology and Trends	29	15/02/2020
3	Recent Developments of the signal processing Techniques in Future Smart Grid	32	08/02/2020
4	Research and Development in Cryptography and Network Security	38	05/02/2020
5	Intellectual Property Rights And Patent Filing	38	27/01/2020
6	Digital Marketing	42	25/01/2020
7	Leadership skills	37	10/12/2019
8	Introduction On Intellectual Property Right	38	09/12/2019
9	IOT automation	34	21/09/2019
10	Research Approches and Statergies of Herbal Formulations	34	19/09/2019
11	Trademark Laws And Changing Its Dimension	38	18/09/2019
12	Analytical Research Methadology of Computer aided Design	32	16/09/2019

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List of Seminars/Workshops

A.Y.2018-19

S.No	Name of the workshop/ seminar/ conference	Number of Participants	Date
1	An Introduction Of IPR With Sound Trade Mark	42	17/05/2019
2	Laws Relating To Patents In India	42	13/03/2019
3	Entrepreneurship in food and Beverage	42	09/03/2019
4	Developing Research skills in application of Gene-Expansion Programming (GEP) for the simplifying the complex equation in water Resources and Irrigation	31	08/02/2019
5	Research Methadology of Data Mining and it's apllications	37	28/10/2019
6	Indian Scenario Of IPR	41	19/11/2018
7	Smart Manufacturing	43	10/10/2018
8	Research Methadology of Nano Formularies and Product Development	28	22/09/2018
9	Research Development in Google cloud Messaging	36	19/09/2018
10	IPR With Copy Rights In Computer Programme	34	18/09/2018
11	Automation and Robotics	37	17/09/2018
12	Social Entrepreneurship	33	10/08/2018
13	Intellectual Property Rights With Focus On Copy Right	33	18/07/2018
14	Importance of IPR of modern global economic environment	38	17/02/2018

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HYBRID ADDER AND MULTIPLIER BASED FIR FILTER DESIGN FOR COMMUNICATION APPLICATIONS

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ABSTRACT: In this project hybrid adder and multiplier based FIR filter design for communication applications is implemented. The adaptive filter has high throughput whose filter coefficients changes during runtime. The main advantage of FIR Filter is its high computational efficiency. Initially input data is given to D-Flip flop. after that data is shifted in row format. next H-adder and H-Multiplier will perform the addition and multiplication operations. To save this outcome of the system memory controlled filter coefficient is used. PRPG is used to arrange the data in pseudo random pattern and because of this there speed of operation will increases. Hence this project will improve the efficiency in effective way.

KEY WORDS: Analog Filter, Digital Filters, Adaptive Filter, Reconfigurable FIR filter, Memory controlled filter coefficient, PRPG (Pseudo Random Pattern Generator).

I.INTRODUCTION

Each filter in DSP has its own characteristics such as low-pass and high-pass have different type of frequency responses. The parameters like gain, stop-band attenuation, roll-off and oscillations in the responses are different for each filter. All these parameters do not match perfectly with the ideal response characteristics like infinite attenuation in stop-band, faster roll-off and unity pass band gain [1]. In order to obtain ideal characteristics filters optimized using approximation functions in designing of analog linear filter. These approximation functions use statistical methods to optimize the transfer function of the filter being designed. The remarkable characteristics of digital filters in their performance lead to widespread use of them in digital signal processing units.

The two main functions performed by filters in DSP are signal separation and restoration.

If a signal mixed up with interference from other signals or noise, signal separation would be better choice [2]. For instance, a device recording heart beat of a fetus in the womb. The actual signal interfered by the heartbeat or air inhalation of the mother. In this case, a filter is employed to separate original signals from interfered signals. Therefore, they can be processed separately.

Sometimes signals may lost or distorted due to unusual reasons. In this case, a filter is used to restore the lost signals. Some examples of signal distortion are sounds recorded from a voice recorder of poor standard, blurring of images captured due to imperfect focusing of lens or shaking. The signals distorted in these cases would have been improved using signal restoration filters. Any one of the filter types either analog or digital filters can address this problem [3].

There are many ways for designing of digital filters. Each filter design is suitable for particular application in time-domain or in frequency domain. Filters for the time-domain applications are specially designed to conserve the signal shape because the information is encoded in the signal by the source. Therefore, filters in this domain are employed to preserve the shape of waveforms like signal restoration, suppressing of DC components and smoothing.

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Development and validation of a RP-HPLC Method for the Estimation of Remdesivir in Bulk and Pharmaceutical Formulation

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ABSTRACT

A simple, reproducible and efficient reversed phase high performance liquid chromatographic (RP-HPLC) method has been developed for estimation of the broad-spectrum antiviral prodrug, Remdesivir in raw material and its injection dosage form. Separation was done by using mobile phase consisting of Acetonitrile : 0.1% Triethylamine, TEA (70:30). The separations were carried out on a Column X-Bridge phenyl (150x4.6mm, 3.5µ) at a flow rate of 1 mL/min. The injection volume was 10 µl and the peaks were detected at 235 nm. The linear dynamic response was found to be in the concentration range of 50µg/mL-300µg/mL and coefficient of correlation was found to be 0.9989. The %RSD value was below 2.0 µg/mL for intraday and interday precision indicated that the method was highly precise. The LOD and LOQ were found to be 6.0 µg/mL and 20 µg/mL respectively which revealed that the method was highly sensitive. The percentage recovery value was higher than 100 %, indicating the accuracy of the method and absence of interference of the excipients present in the formulation. The proposed method was simple, fast, accurate, precise and reproducible and hence can be applied for routine quality control analysis of Remdesivir in bulk and pharmaceutical formulation.

Keywords: Remdesivir, Estimation, Injection, RP-HPLC.

INTRODUCTION

Remdesivir is a broad-spectrum antiviral medication. It is administered via injection into a vein. During the COVID-19 pandemic, Remdesivir was approved or authorized for emergency use to treat COVID-19 in numerous countries. Remdesivir was originally developed to treat hepatitis C[17], and was subsequently investigated for Ebola virus disease and Marburg virus infections[18] before being studied as a post-infection treatment for COVID-19[19]. Remdesivir is a prodrug that is intended to allow intracellular delivery of GS-441524 monophosphate and subsequent biotransformation into GS-441524 triphosphate, a ribonucleotide analogue inhibitor of viral RNA polymerase[14].

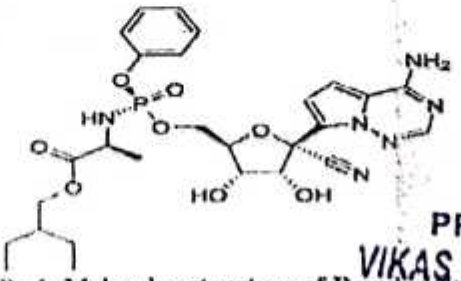

Fig 1: Molecular structure of Remdesivir

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Design_of_Efficient_32-bit_Vedic_Multiplier

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Abstract: Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluatedon the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. Its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation.Power dissipation is another important constraint in an embedded system which cannot be neglected.

In this paper we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic, which is the first of its kind. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications.For arithmetic multiplication, various Vedic multiplication techniques like Urdhva tiryakbhyam, Nikhilam and Anurupye has been thoroughly discussed. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay formultiplication of all types of numbers, either small or large.Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3E kit have been done.

Keywords- Urdhva Tiryakbhayam,Fast Fourier Transforms (FFTs),Vedic multiplier..

1.Introduction: A Multiplier is an electronic circuit used in digital circuits, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. In digital circuits multiplying to binary numbers is done using repeated addition using full adders and half adders. A multiplier is used in many applications such as image processing, signal processing, microprocessors, and microcontrollers, etc.

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Design & Implementation of Triple Bit Error Correcting Bch Decoder with High Efficiency for Emerging Memories

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Date of Submission: 20-11-2021 Date of Acceptance: 05-12-2021

ABSTRACT: As the technology scales down emerging memories struggling with reduced reliability. As a solution error-correcting code ECC and its decoder circuits have been applied. To correct two (or) three errors BCH code is widely adopted. We have double- error-correcting and triple error-detecting (DEC-TED) bose-Chaudhuri–Hocquenghem (BCH) code decoder with high decoding efficiency and low power for error correction in emerging memories. Here we are implementing triple bit error correcting (TEC) decoder to increase the decoding efficiency, we propose an adaptive error correction technique for the BCH codethat detects the number of errors in a codeword immediately after syndrome generation and applies a different error correction algorithm depending on the error conditions. With the adaptive error correction technique, the average decoding latency and power consumption are significantly reduced owing to the increased decoding efficiency. To further reduce the power consumption, an invalid-transition-inhibition technique is proposed to remove the invalid transitionscaused by glitches of syndrome vectors in the error- finding block.

Keywords: adaptive error correction, bose-Chaudhuri–Hocquenghem (BCH) code, double error correcting (DEC)and triple error detecting & correcting (TED -TEC), emerging memories, error correcting code(ECC),LUT-, based decoders, invalid-transition- inhibition technique

I. INTRODUCTION

Emerging memories, such as phase change memory, spin-transfer torque magneto resistive random accessmemory (STT-MRAM), phase change RAM (PRAM), andresistive random access memory (ReRAM) have been investigated to fill the gaps in terms of performance and density between DRAM and NAND flash memory,referred to as storage class memories (SCMs). They are of interest for their flexible and efficient memory hierarchy, owing to their nonvolatile, high-density, and low-latency characteristics [1]. In addition to SCMs, some emerging memories, such as STT-MRAM, are also considered promising candidate embedded memories due to their fast read and write latencies, low leakage power, and logic-friendly compatibility [2]–[3]. As technology scales down, these emerging memories arealso struggling with reduced reliability, and as a solution, error-correcting code (ECC) and its encoder/decoder circuits have been applied. While NAND flash requires a powerful ECC capable of correcting up to 100 errors, most of the emerging memories can reach the required chip yield using an ECC capable of correcting two or three errors because of new developments in storage physics [2]–[8]. In addition to simply increasing the memory yield, ECC can be used to optimize memory performance regarding density [9], [10] and energy consumption [11], [12]. In this manner, ECC has become an essentialpart of emerging memories. To correct two or three errors, the Bose–Chaudhuri–Hocquenghem (BCH) code is widely adopted for emerging memories [2]–[8]. However, the standard iterative and sequential decoding processes, which require multiple cycles, are not compatible with emerging memories. This is because the latency of the BCH code decoder should be a few nanoseconds, considering the short read or write access time in emerging memories. To achieve a double-error-correcting (DEC) BCH code decoder withlatency of a few nanoseconds, a fully parallel decoder structure thatuses combinatorial logic gates has beenproposed in [13]–[17]. However, it continues to have 50%–80% latency penalty and consumes 6–8 times more power than the single-error-correcting and double-error detecting (SEC-DED) decoder. As non- or single-bit errors are considerably more likely than multi bit (double-bit or triple bit) errors despite the increased raw bit-error rate (RBER) in nanotechnology, it is inefficient to deal with non- or single bit errors with a DEC-TED decoder in terms

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DESIGN AND IMPLEMENTATION OF HIGH EFFICIENT DELAY UTILIZATION OF (n/2) PARALLEL MULTIPLIER

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ABSTRACT: In this paper, design and implementation of high efficient delay utilization of (n/2) parallel multiplier is done. Basically, multipliers are key arithmetic circuits in many of these applications including digital signal processing (DSP). This n/2 parallel multiplier uses adder that limits its carry propagation. First the alignment of partial products generator will be done. After that partial products takes this registers and generates the propagate and generate signals. After this n/2 × n/2 multiplication operation is performed. Now this bits perform the addition operation and gives the final product. Hence this paper reduces the delay in effective way.

Key Words: VLSI, Digital signal processing (DSP), Partial products, Multiplexer and Adder.

I. INTRODUCTION

Basically, in communication systems like error correction codes and cryptography, finite field is most widely used. Arithmetic operations are performed using the field elements. Two basis are normally used to implement a system that is normal basis and polynomial basis. Normal basis is used to implement the hardware and perform the low cost squaring operations. In the same way, polynomial basis is used to implement the software and in the same way this also performs the low cost squaring operations [1]. Accuracy could be compromised to a defined extent in most of the present-day applications like image recognition and processing. Multiplier is the basic building block of such applications which involve a lot of mathematical processing. This leads to a win-win balancing between the energy consumed by the circuit and the required accuracy.

The energy consumed by any system is directly proportional to the multiplication accuracy of those systems. If a system requires high accuracy then it consumes more energy and vice versa. Also, there could be section or module of that systems which needs lesser accuracy than other parts of the system. If the accuracy is kept constant across all such modules it greatly increases the amount of energy consumed by the overall system. However, if the accuracy of the multiplier is characterized to change as per the need of that particular module or section of the entire system, this would have a great impact in reducing the amount of energy consumed by the system [2].

This method of configuring and adjusting the accuracy of a multiplier based on the requirement of the system or application is achieved using different adder sub module of the multiplier module to characterize the accuracy based on the approximation technique. There should be reconfigurable multipliers in various program stages or applications [3]. So, in this paper we designed a multiplier which has an accuracy decided on the go based on the requirement of the application.

Montgomery's multiplier is classified into three types, they are bit-serial, bit-parallel, and digit serial architectures. Bit-parallel shape is rapid; however it's far steeply-priced in phrases of vicinity. Bit-serial structure is region efficient, but it's far too sluggish for plenty packages. The digit-serial structure is flexible which may change the space and velocity, consequently, it

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Implementation of 32*32 Dadda Multiplier

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ABSTRACT: In this research paper, the technique for the design of a fast multiplier is proposed by using two different techniques. A 4:2 compressor is used for power-efficient row compression in the proposed model, whereas for faster final summation, a carry-select adder has been used. Based on the above technique, a 16-bit Dadda-multiplier is proposed and its performance is analysed by comparing it with the standard 16- bit Dadda-multiplier which normally uses carry-look ahead adder. The time delay of carry-select adder is improved when compared to carry propagate adder. The result depicts that the proposed 16-bit Dadda-multiplier is 4.85% power efficient and 63.4%-time delay is improved. The simulation of the proposed multiplier is carried out using Verilog HDL in Xilinx ISE Design Suite 14.7.

Keywords— ALU, Dadda-multiplier, 4:2 compressor, carry select adder, carry propagate adder, Wallace-multipliers, half adder, full adders

I. INTRODUCTION

Multiplier is one of the most important circuits for designing computers and computing devices. The Dadda technique for partial product reduction is based on the idea of 'avoid use of full adder.' But the use of full adder is more regular in other Wallace tree multipliers. This paper presents a modified Dadda technique based on the idea of 'prefer the use of full adder over the use of half adder.' Only the last stage that is 'three to two reductions' is the exception. This idea used in the modified technique makes it more regular and simple. Hence, based on the idea, it is named as 'Full-Dadda.' The fact behind saying this technique an alternative approach is that this technique results in same number of full adders, half adders, same size of final carry propagation adder and same number of compressors (adders) at each stage as required in the Dadda technique. Therefore the proposed multiplier can be used in place of Dadda multiplier in all its applications. This paper presents a comparative performance analysis of the proposed multiplier with the Dadda multiplier. For this comparison each multiplier with different operand sizes is taken. The main disadvantages of the Dadda multiplier are: (i) it is less regular, (ii) more complex and (iii) it reduces less number of bits at early stages of reductions. The proposed 'Full-Dadda' multiplier is more regular, simple and reduces more number of bits at early stages of summand reduction. In section 2, there is brief overview of literature and in section 3; there are general rules and equations for reduction scheme and number of hardware components respectively. The comparison between multipliers is arranged in five sub-sections under section.

DESIGN A HIGH SPEED EFFICIENT VLSI ARCHITECTURE OF E.R HYBRID ADDER

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ABSTRACT: In this paper the Design a high speed efficient VLSI architecture of E.R Hybrid adder is implemented. Basically, adders are most commonly used in the applications of digital signal processing's, Microprocessors etc. Hybrid adder performed in three stages, they are propagator and generator stage, Internal carry generation stage and final sum stage. In this propagator and generator signals are generated by using propagation stage. Internal Carry generation stage will generate the carry. If any errors are occurred then error detection stage will detect the errors and error recovery stage will recover those output values. Final sum stage will take the output of hybrid adder and performs the operation and gives sum as output. At last from results it can observe that the propose system gives effective results.

KEY WORDS: Hybrid Adder, Internal Carry generation Stage, Final Sum Stage, propagator, Generator, VLSI.

I. INTRODUCTION

Fastest technologies are developed in present days. In present days, reduction of device size, fast operation and low power consumption are required. The designing of low power VLSI system has more demand in mobile communication. Due to the device designed by designer with high speed, low power consumption and small silicon area, the device is available with low power.

ALU (Arithmetic logic unit) and FU (Floating point unit) are the main parts in computations [1]. Logical computations are addition, subtraction, multiplication, division and logical operations are AND, OR, INV and comparison which are processed by Arithmetic logic unit (ALU). Data path has an important role in digital signal processors and microprocessors because of some characteristics such as power consumption, speed of operation and die-area.

Data path contains complex operations are subtraction, addition, division and multiplication [2]. The main important factor is data path performance which is affected by efficient hardware units of complex computations. In the data path addition is the important executed operation, addition operation contains binary adder to add given numbers. In complex computations such as decimal operations, multiplication and division, adders has important task [3]. To get data path efficiently, the implementation of binary adder should be efficient.

In central processing unit (CPU) crucial element is ALU (Arithmetic logic unit). An adder has important function in ALU and an adder performs not only addition but also performs multiplication, subtraction and decrement/increment. In ALU and general processors to get better performance, efficient adder is needed. From 1950s, for hardware implementation of VLSI arithmetic circuits, research started on efficient adder implementation. In control systems and digital signal processing main operation is the addition.

The properties of system or processor like accuracy and speed depends upon the performance of adder. To execute the addition of numbers, adder is used which is a digital circuit. Different processors and computers contains ALU in which adder is used. To reduce different parameters, different designs have been implemented based on parallel and serial structures. Four elementary operations are performed in binary addition.

The adders can be represented in many forms like BCD (binary coded decimal)

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DESIGN A HIGH SPEED RIFFA BASED HOMOMORPHIC ENCRYPTION/DECRYPTION

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ABSTRACT: In this project, design and implementation of high speed and high secure BFC based Homomorphic encryption is done. This system will provide better security and resource efficiency compared to existing standards. RIFFA based homomorphic encryption technique guarantee both privacy and integrity. The main intent is to increase the speed of operation. Initially, input bits and key is expanded serial by using PCIe. Next, bits are substituted using S-Box. After substitution of bytes, the bits will be reusable using RIFFA. After reusable procedure shifting operation is performed. Now these bits are encrypted. Similarly, decryption process is reverse to this operation.. Hence RIFFA based homomorphic encryption and decryption is implemented and it gives better security compared to exist one.

KEY WORDS: Homomorphic encryption, Large Integer Multiplication, Operand Reduction, VLSI Architecture, S-Box, Peripheral Component Interconnect express (PCIe), Reusable Integration Framework for FPGA Accelerators (RIFFA).

I. INTRODUCTION

Fully Homomorphic Encryption is for the most part utilized in the database of the board frameworks (DMBS). One of the present issues related with the utilization of databases is the test of verifying and securely putting away the legitimate treatment of classified information in the remote database. Privacy of touchy data can be guaranteed using cryptography.

It may, be the utilization of industrious encryption calculations to store the data in remote databases can fundamentally decrease the presentation of the framework without interpreting. To take care of the issue, in MIT examines exhibited Crypto system.

Utilizing additively homomorphic crypto framework enables the server to execute SUM, AVG, and Count Questions over encoded information; the other SQL inquiries utilize the distinctive encryption calculations with the vital usefulness. The adjustment of completely homomorphic cryptosystem will keep the capacity to perform run of the mill database tasks on encoded information without decoding the information in a confided condition. In any case, such a cryptosystem must fulfill certain prerequisites for practical qualities and computational unpredictability, which is significant.

Fully Homomorphic Encryption (FHE) is a huge achievement in cryptographic research in recent years. A FHE plan can be utilized to elective perform calculations on figure content without trading off the substance of relating the plain text [1]. Therefore, a practical FHE plan will open the way to various new security advances and protection related to the applications, for example, security safeguarding pursuit and cloud-based processing. For the most part, FHE can be ordered into three classifications: cross section based, number based, and learning with mistakes.

One of the fundamental difficulties in the improvement of FHE applications is to moderate the amazingly high-computational intricacy and asset necessities [2-4]. For instance, programming usage of FHE in superior PCs still expend the critical calculation time, especially to achieve the vast whole number duplication which more

AREA EFFICIENCY ADAPTIVE SARADC WITH THE IMPROVEMENT IN LINEARITY OF POWER OPTIMIZATION

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Abstract: The analysis of area efficient conventional binary-weighted and switched-capacitor DAC with the split topology capacitor for adaptive SARADC to improve the power linearity of power optimization is presented in this paper. Even though the reduction of DAC's area will be the major cause for the usage of the spilt-capacitor topologies which is presented in the analysis that, it is not always the case since the linearity parameters of topologies of split capacitors are more sensitive to the parasitic effects. Depending on two methods of switching mechanism, such as V_{cm}-based switching and redistribution of the conventional charge, a adaptive successive approximation registers (SAR) analog-to-digital converters (ADC) linearity analysis using a split DAC structure is presented in this paper. The integral nonlinearity and differential nonlinearity are called as static linearity. The analysis of performance on the static linearity and spilt DAC with parasitic effects are considered here. Some of the results of measurement are speed power as well linearity that clearly shows the advantages of using V_{cm} - based switching.

Key words: Switched capacitor DAC, adaptive SARADC, Linearity analysis and split DAC

I. INTRODUCTION

Successive approximation register analog-to-digital converters (SARADC) [1] are widely used in low power and medium-resolution applications such as medical implant devices [2], wireless sensor networks, [3] etc. One of the key elements of every adaptive SARADC is the digital-to-analog converter (DAC).

The DAC in SARADC is usually based on the switched resistors network, switched current sources network or switched capacitors network. The latter is convenient for low power applications since it does not consume static power like the former ones.

Also, the switched capacitor DAC network can be used as the sample and hold circuit in the sample phase. Differential realizations of SARADC, compared to single-ended realizations, is more resistant to noise and other effects which reduce the ADC's performance such as charge injection. These realizations require two switched capacitor arrays: one for positive, and another for negative comparator input which can increase the chip area.

This paper analyzes the conversion non-linearity, induced by supply noise, switching methods, and parasitic effects in adaptive SARADCs. The static nonlinearities based on the conventional and V_{cm}-based [4] switching methods are theoretically analyzed, and the mathematical models are developed to verify the effectiveness of the V_{cm}-based approach. SARADC with V_{cm}-based switching demonstrates the performance profits in terms of speed, power, and linearity by using V_{cm}-based switching [5]. There are multiple studies on capacitor array topologies, and switching algorithms [6], [7] that discuss converter's linearity, energy efficiency, area problems and performance. The SARADC's

DESIGN SRAM EMULATION WITH PRECHARGE USING ERROR CHECK BITS

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ABSTRACT: Modern ICs are enormously complicated due to decrease in device size. For high-speed memory applications such as cache, a SRAM is often used. In this paper SRAM is designed with pre charge bits using error check bits. The memories can be protected with check bits to detect errors. Single-bit errors corrected when memories are protected with check bit. by employing the gated pull down path and boosting scheme, search speed will be increased. By considering the number of mismatch and discharging speed, the discharging is adaptively controlled in the proposed system. At last the proposed system gives effective results in terms of speed and delay.

KEY WORDS: SRAM (static random access memory), pre charge unit, check bits, content addressable memory, error correction and location schemes.

I.INTRODUCTION

As CMOS innovation downsizes to nano scale and recollections are joined with an expanding number of electronic frameworks, the delicate mistake rate in memory cells is quickly expanding, particularly when recollections work in space conditions due to ionizing impacts of barometrical neutron, alpha-molecule, and enormous beams. Albeit single piece upset is a noteworthy worry about memory unwavering quality, multiple cell upsets have turned into a genuine dependability worry in some memory applications. So as to make memory cells as issue tolerant as could reasonably be expected, some error correction codes (ECCs) have been generally used to secure recollections against delicate mistakes for quite a long time. For instance, the punctured different set codes have been utilized to manage MCUs in Recollections. Yet, these codes require more area, power, and delay overheads. Since the encoding and unraveling circuits are increasingly in these confounded codes [1-2].

The general thought for accomplishing blunder location and adjustment is to include some excess (i.e., some additional information) to a message, which recipient can use to check consistency of the conveyed message, and to get information resolved to be degenerate. Mistake identification and redress plan can be either methodical or non-efficient. In a deliberate plan, the transmitter sends the interesting information, and connects a fixed number of check bits (or equality information), which are gotten from the information bits by some deterministic calculation. On the off chance that just the mistake discovery is required, a recipient would simple be able to apply a similar calculation to the got information bits and contrast its yield and the get check bits; if the qualities don't coordinate, a blunder has happened sooner or later all through the transmission [3].

Error correcting codes are normally utilized in lower-layer correspondence, As well with respect to solid stockpiling in media, for example, CDs, DVDs, hard plates and RAM. Static RAM based Field-Programmable Gate Arrays (FPGAs) are most broadly utilized in assortment of utilizations chiefly because of brief time-to market time, adaptability, high thickness, and cost-proficiency. SRAM-based FPGA stores rationale cells arrangement information in the static memory composed

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PAPER

Experimental optimization of mechanical properties of Al7010/B_4C/BN hybrid metal matrix nanocomposites using Taguchi technique

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Keywords: mechanical properties, Taguchi technique, ANOVA, B_4C, BN, ultrasonic assisted stir casting

Abstract

The composite material properties largely dependent on the processing methods and the parameters employed during their manufacturing. In the present study, the effect of B_4C and BN nanoparticles on tensile strength and microhardness of Al7010 hybrid metal matrix nanocomposite is investigated. The composite is prepared using ultrasonic assisted stir casting technique, and the effect of processing parameters like weight percentage of particles, stirrer speed, stirring time and temperature on ultimate tensile strength and microhardness are optimized using Analysis of Variance technique. The experiments are planned using Taguchi design of experiment based on the L_{25} orthogonal array. In all the input parameters, the wt% of B_4C and BN is most significant on ultimate tensile strength and microhardness followed by other parameters. Further, the verification of optimal experimental results the confirmation tests was conducted and also a percentage error is found.

1. Introduction

In modern days, the production of aluminium metal matrix composites (AMMCs) involves the addition of ceramic particles into aluminum and its alloys. The AMMCs exhibit many winsome mechanical properties like high stiffness, poor density, low ductility, poor fracture toughness, excellent strength and better corrosion resistance. The AMMCs are extensively used in marine, military, aerospace and automobile industries etc [1]. The aluminium metal matrix nanocomposites reinforced with ceramic nanoparticles into the aluminium matrix improve the ductility, fracture toughness and increased mechanical strength. The ceramic hard particles like B_4C, TiB_2, SiC, WC, ZrB_2, BN, etc., are used as reinforcements in AMMCs. Among these reinforcement particles, B_4C particles possess outstanding bonding characteristics with aluminum and have low density (2.52 g cm^{-3}), excellent strength, good wear resistance and hardness, high melting point and is used as replacement for SiC and Al_2O_3 [2, 3].

The aluminium hybrid metal matrix nanocomposites (AHMMNCs) possess extraordinary mechanical properties such as high strength, poor density, low coefficient of thermal expansion, high ductility and toughness. It was formed by a combination of more than one different nano particle reinforced into the aluminum matrix to improve the toughness, ductility, decrease machining difficulties and improve wear resistance [4]. The nano boron carbide particles mixed with the aluminium matrix increases the mechanical strength and wear resistance of the composites (AMMNCs) and boron nitride nano particles is a potent reinforcement and acts as a solid lubricant and improves the toughness, wear resistance and acts as a self-lubricant in the AMMNCs [5]. Harichandran *et al* produced AHMMNCs with nano sized B_4C and BN as reinforcement materials in the aluminium alloy using ultrasound assisted stir casting. The tensile strength of the composite is improved by 67% compared to the base alloy. The B_4C nanocomposite addition with 6 wt% B_4C

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ANALYSIS OF MONO LEAF SPRING

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ABSTRACT

In general springs are used to absorb shocks and to prevent the vibrations. Even though various types of springs are available in the market. Leaf springs are plays a major role in the automobile industry. The objective of this present work is to estimate deflection, stress and mode frequency induced in the mono leaf spring of a lorry .The Leaf was modeled and analysis were carried out on Steel and Composite materials (E glass epoxy and carbon epoxy) for both. The results show that by using the composite Leaf, We can reduce the stresses induced in the member. After comparing Results Composite Leaf has less stresses and will been added advantage to use leaf springs in Automobile industries. Replacing of conventional springs with composites reduces the total weight of the body and hence power consumption could be reduced and Life is Increases.

Keywords: *Leaf Spring,Pro-E,Ansys-13.*

I. INTRODUCTION

A spring is defined as an elastic body, whose function is to distort when loaded and to recovers its original shape when the load is removed. Semi- elliptic leaf springs are almost universally used for suspension in light and heavy commercial vehicles. For cars also, these are widely used in rear suspension. The spring consists of a number of leaves called blades. The blades are varying in length. The blades are us usually given an initial curvature or cambered so that they will tend to straighten under the load. The leaf spring is based upon the theory of a beam of uniform strength. The lengthiest blade has eyes on its ends. This blade is called main or master leaf, the remaining blades are called graduated leaves. All the blades are bound together by means of steel straps. The spring is mounted on the axle of the vehicle. The entire vehicle rests on the leaf spring. The front end of the spring is connected to the frame with a simple pin joint, while the rear end of the spring is connected with a shackle as show in fig1.1

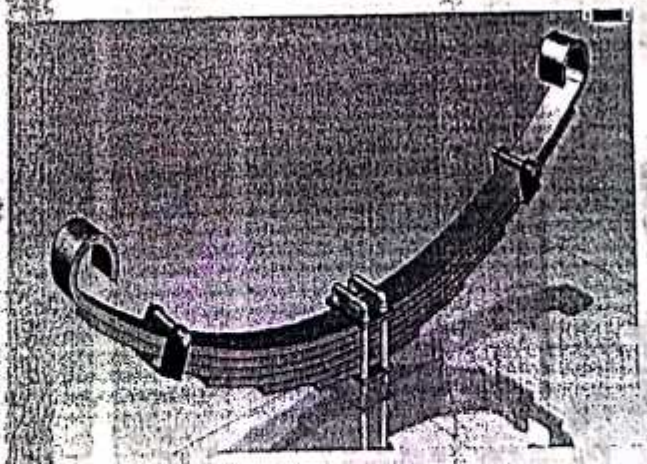

Figure 1: Leaf Spring

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EXPERIMENTAL ANALYSIS OF DOUBLE PIPE HEAT EXCHANGER BY USING NANO – FLUIDS AL_2O_3& SIO_2

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ABSTRACT

In this research work forced convection flows of Nano-fluids consisting of water with Nanoparticles $AL_2O_3$and SIO_2in a horizontal tube with constant wall temperature are investigated numerically. A single-phase model having two- dimensional equations is employed with either constant or temperature dependent properties to study the hydrodynamics and thermal behaviors of the Nano-fluid flow. The velocity and temperature vectors are presented in the entrance and fully developed region. The variations of the fluid temperature, local heat transfer coefficient and pressure drop along tube length are shown in the paper. Numerical results shows that the heat transfer enhancement due to presence of the Nanoparticles in the fluid in accordance with the results of the experimental study used for the validation process of the numerical model.

Keywords: CSTR-PID-ZN-Fuzzy-MRAM-MATLAB.

I. NANO FLUID PREPARATION METHOD

1.1 Two-Step Method

This is the most widely used method for preparing Nano fluids. Nanoparticles, Nano fibers, Nanotubes, and other Nano-materials used in this method are first produced as dry powders by chemical or physical methods. After that the Nano sized powder is to be dispersed into a fluid in the second processing step with the help of intensive magnetic force agitation, ultrasonic agitation, high-shear mixing, homogenizing, and ball milling. Two-step method is the most economic method to produce Nano fluids in large scale, because Nano powder synthesis techniques have already been scaled up to industrial production levels. Due to the high surface area and surface activity, Nanoparticles have the tendency to aggregate. The important technique to enhance the stability of Nanoparticles in fluids is the use of surfactants. However, the functionality of the surfactants under high temperature is also a big concern, especially for high-temperature

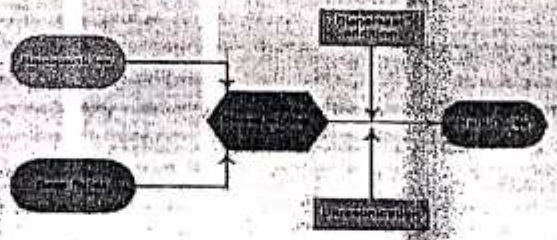

Fig 1.1.1 Two-Step Mixing Procedure Diagram of Nano- Fluid

Due to the difficulty in preparing stable Nano fluids by two-step method, several advanced techniques are developed to produce Nano fluids, in one-step method.

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VIBRATION ANALYSIS OF CARBON NANOTUBE REINFORCED COMPOSITE USING ANSYS

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ABSTRACT

The energy crisis and global inclination to reduce green house gas emissions have been catalytic in directing the attention of research scientists to look for light weight materials with high strength .Composites are the ones with this kind of exceptional properties .The emergence of Carbon Nanotubes has created new opportunities for fabrication of polymer composites that possess strong potential for a wide spectrum of the applications .The one-dimensional structure of carbon nano tubes has a very high anisotropic nature and unusual mechanical properties, which made them as promising nano filler for the composite structures. The primary focus currently is to develop new generation of Nano-composite materials capable of exhibiting good combination of properties .The present research work is focused on the evaluation of mechanical properties like Young's modulus and also to investigate the natural frequency of nano particle reinforced composites through Finite Element Analysis. The Vibration test is carried out to get the information of the first mode shape of this discrete Nano composite, and this is used to further estimate the mode shapes in the composite for different end conditions and also, to check this composites performance in real time situations using the probable cuts in the model and this procedure is done by using ANSYS Pack.

Keywords: Composite: a material made from two or more constituent materials..

I. INTRODUCTION

Composite comes from a Latin word commoner means to put to gether. A composite material consists of two or more constituent materials with significantly different properties combined together at a macroscopic scale with a recognizable interface between them, to produce a material with characteristics different from its constituents. Nature itself has a number of Composite materials like Wood, human bone, Bamboo etc. The Composites are classified into different types based on the matrix and reinforcement materials.

II. PROBLEMOBJECTIVE

The objective of the present work is to analyze the vibration of carbon nano tube reinforced composite using ANSYS to utilize it in industries. First we have to find the Elastic properties of the CNT reinforced composite which is having spherical shape particles of micron diameter as reinforcement in the epoxy resin as matrix..And to find the first Natural frequency of the SWCNT reinforced composite .Now we have to model and simulate for different boundary end conditions and see the vibrational behaviour of the 1,2 and 3 wt% CNT reinforced composite at these conditions .And finally we have to find the Natural frequency of the SWCNT reinforced composite which is having a irregularity in itsshape.

III. RESULTS ANDDISCUSSION

Micro mechanical analysis of swcnt reinforced composite

The Elastic properties of composites are evaluated effectively by adopting Representative Volume Element (RVE) that consist of a single spherical particle surrounded by matrix material and is One-eighth portion is considered for analysis as shown in Figure 3. 1. Due to the spherical shape of the nanotube, the cubic shape unit cell is considered for the analysis.

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THERMO ELASTIC BEHAVIOUR OF A THIN HYBRID FOUR-LAYERED FRP SKEW CROSS-PLY LAMINATES WITH CIRCULAR CUTOUT

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ABSTRACT

The present paper deals with the prediction of thermo elastic behaviour of the thin four-layered Cross-ply Hybrid Fibre Reinforced Plastic (FRP) skew laminated composite plate with circular cut out by considering two composite materials Graphite- Epoxy and Boron-Epoxy materials which are subjected to uniform pressure load and thermal loading. The problem is modeled by using ANSYS software based on the Classical Lamination Theory (CLT) which is suitable for the analysis of thin laminates with circular cut-out. The effect of size of the circular cut out and skew angle on the stresses are shown for Cross and Angle-ply laminates. The principle stresses and shear stresses are evaluated for different cross sections. The present analysis is useful for the safe and effective design of the skew laminates with circular cut out under uniform pressure load and thermal load conditions.

Keywords: *hybrid FRP, Skew laminate, Finite element analysis, cross-ply , classical theory, thermal stresses. Circular cut out.*

I. INTRODUCTION

A composite material is made by combining two or more materials – often ones that have very different properties. The two materials work together to give the composite unique properties. However, within the composite you can easily tell the different materials apart as they do not dissolve or blend into each other. Most composites are made of just two materials. One is the matrix or binder. It surrounds and binds together fibres or fragments of the other material, which is called the reinforcement. The first modern composite material was fibreglass. It is still widely used today for boat hulls, sports equipment, building panels and many car bodies. The matrix is a plastic and the reinforcement is glass that has been made into fine threads and often woven into a sort of cloth. On its own the glass is very strong but brittle and it will break if bent sharply. The plastic matrix holds the glass fibres together and also protects them from damage by sharing out the forces acting on them. Some advanced composites are now made using carbon fibres instead of glass. These materials are lighter and stronger than fibreglass but more expensive to produce.

They are used in aircraft structures and expensive sports equipment such as golf clubs.

Statical and dynamical behaviour of thin fibre reinforced composite laminates with different shapes Based on the classical laminated plate theory [1] Thermal buckling analysis of symmetric and antisymmetric cross-ply laminated hybrid composite plates with an inclined crack subjected to a uniform temperature rise [2] , buckling of functionally graded plates (FG plates) with an elliptical cut out under combined thermal and mechanical loads is investigated using Finite Element Method [3] The free vibration analysis of laminated composite skew plates with delamination around a centrally located quadrilateral cut out is carried out based on the high-order shear deformation theory (HSDT) [4] the prediction of interlaminar stresses in simply supported laminated FRP composite plate with a circular cut-out under transverse load using 3-D finite element analysis [5] the free vibration analysis of a thin Fibre Reinforced Plastic (FRP) skew laminated composite plate with a circular cut-out at the geometric centre [6] the interlaminar stresses are predicted for a bidirectional skew laminated unidirectional continuous fibre reinforced plastic (FRP) composite with a circular cut out at the geometric centre of the plate using three dimensional finite element method with geometric nonlinear option [7].

The present investigation intends to apply the finite element technique, based on classical lamination theory, for the analysis of symmetric and anti-symmetric thin laminates under uniform pressure load and thermal loading

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FLOW AND HEAT TRANFER ON ALCOHOL IN MICRO-CHANNEL

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ABSTRACT

The objective of the current experimental program is to generate data for liquid flow through micro-channels. The channel dimensions are 1.5 mm deep x 0.75 mm width. Rectangular 47 micro-channels were cut on a stainless steel substrate (230 mm x 160 mm) by Electro Discharge Machining (EDM) technique. The use of micro channels is recent topic of investigation. Micro channels are used to remove high heat fluxes from smaller area. Such as electronic components like printed circuit board (PCB), chip space, laser applications etc. It is proposed to design and fabricate micro channels and to study the heat transfer characteristics, such as heat flux, liquid temperature, wall temperature and Nusselt number correlation. However, the single phase forced convective heat transfer and flow characteristics of alcohol in micro channels structures plates with small rectangular channels and distinct geometric configurations are to be investigated experimentally. Finally, experimentally obtained values will be compared with the theoretical or predicted values.

Keywords: Experiments, Laminar, Friction factor, Nusselt number and Micro-channels.

Nomenclature

C	empirical constant {no units}
c_p	specific heat, J/kg-K
d	diameter, m
f	friction factor, {no units}
H	height of the channel, m
h	heat transfer coefficient, W/m²-K
k	thermal conductivity, W/m-K
l	length of the channel, m
$\dot{m}$	mass flow rate, kg/s
Nu	Nusselt number, {no units}
p	pressure drop, Pa
Pr	Prandtl number, {no units}
Q	heat transfer rate, W
q"	heat flux, W/m²
Re	Reynolds number, {no units}
T	temperature, °C
v	velocity, m/s
W	width of the channel, m
z	no. of channels

Greek symbols

Δ	Difference
μ	Viscosity, Pa s
ρ	Density, kg/m³

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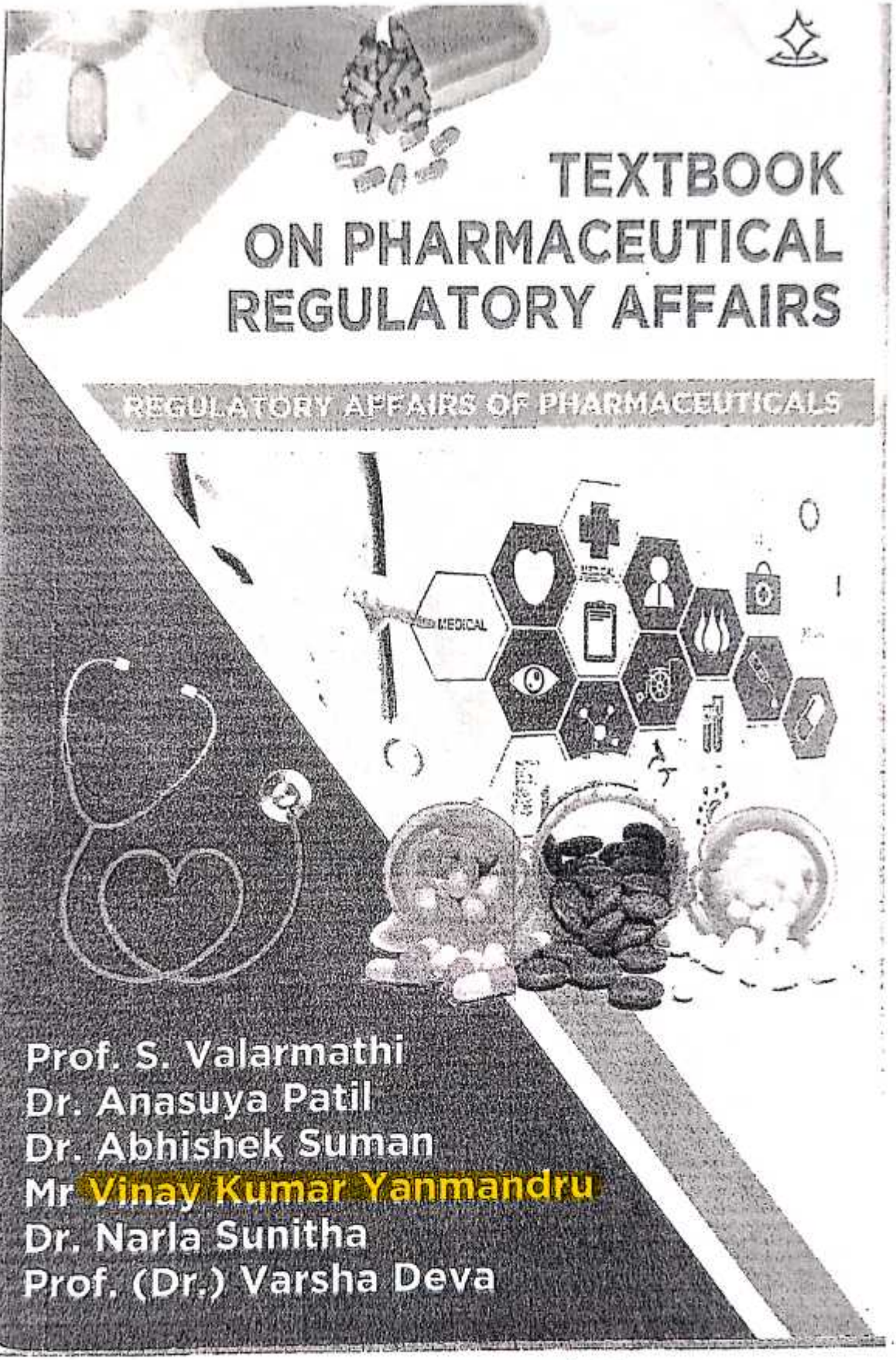

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