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Nunna – 521 212, Vijayawada Rural, NTR District, A.P. India.
Email: principal.9t@gmail.com

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NUNNA - 521 212
Vijayawada Rural, NTR Dist., A.P.

AREA EFFICIENCT ADAPTIVE SARADC WITH THE IMPROVEMENT IN LINEARITY OF POWER OPTIMIZATION

[1]P VENKATESWARARAO, [2]SEKHAR VEMPATI, [3]SARNALA BUTCHI BABU

[1]Assistant professor, Dept of ECE, VIKAS College of Engineering and Technology, Vijayawada rural, Andhra Pradesh. India.

[2]Assistant professor, Dept of ECE, VIKAS Group of Institutions, Vijayawada rural, Andhra Pradesh, India.

[3]Assistant Professor, Dept of ECE, VIKAS College of Engineering and Technology, Vijayawada rural, Andhra Pradesh, India.

Abstract: The analysis of area efficient conventional binary-weighted and switched-capacitor DAC with the split topology capacitor for adaptive SARADC to improve the power linearity of power optimization is presented in this paper. Even though the reduction of DAC's area will be the major cause for the usage of the spilt-capacitor topologies which is presented in the analysis that, it is not always the case since the linearity parameters of topologies of split capacitors are more sensitive to the parasitic effects. Depending on two methods of switching mechanism, such as V_{cm}-based switching and redistribution of the conventional charge, a adaptive successive approximation registers (SAR) analog-to-digital converters (ADC) linearity analysis using a split DAC structure is presented in this paper. The integral nonlinearity and differential nonlinearity ore called as static linearity. The analysis of performance on the static linearity and spilt DAC with parasitic effects are considered here. Some of the results of measurement are speed power as well linearity that clearly shows the advantages of using V_{cm} - based switching.

Key words: Switched capacitor DAC, adaptive SARADC, Linearity analysis and split DAC

I. INTRODUCTION

Successive approximation register analog-to-digital converters (SARADC) [1] are widely used in low power and medium-resolution applications such as medical implant devices [2], wireless sensor networks, [3] etc. One of the key elements of every adaptive SARADC is the digital-to-analog converter (DAC).

The DAC in SARADC is usually based on the switched resistors network, switched current sources network or switched capacitors network. The latter is convenient for low power applications since it does not consume static power like the former ones.

Also, the switched capacitor DAC network can be used as the sample and hold circuit in the sample phase. Differential realizations of SARADC, compared to single-ended realizations, is more resistant to noise and other effects which reduce the ADC's performance such as charge injection. These realizations require two switched capacitor arrays: one for positive, and another for negative comparator input which can increase the chip area.

This paper analyzes the conversion non-linearity, induced by supply noise, switching methods, and parasitic effects in adaptive SARADCs. The static nonlinearities based on the conventional and V_{cm}-based [4] switching methods are theoretically analyzed, and the mathematical models are developed to verify the effectiveness of the V_{cm}-based approach. SARADC with V_{cm}-based switching demonstrates the performance profits in terms of speed, power, and linearity by using V_{cm}-based switching [5]. There are multiple studies on capacitor array topologies, and switching algorithms [6], [7] that discuss converter's linearity, energy efficiency, area problems and performance. The SARADC's

performance depends on multiple parameters like technology parameters, supply voltage, unit capacitors size etc. The detailed analysis of area efficiency of different topologies is presented.

The binary-weighted capacitive DAC is widely used in SAR ADCs. However, the capacitance of the DAC array increases exponentially with the resolution, which imposes larger consumption of switching energy, area, and settling time. A valuable substitute is the split capacitive DAC, which has been recently reconsidered for medium resolution. Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity.

However, by using the metal-insulator-metal (MIM) capacitor or/and DAC mismatch calibrations the split structure can become suitable for a medium-resolution target. On the other hand, the conversion linearity is also directly correlated with the switching sequences of the DAC array where the conventional charge-redistribution switching results in worse conversion linearity and more energy losses.

II. LITERATURE SURVEY

Xing [6] proposed a 7-bit MS/s four-way time interleaved adaptive SARADC. In this paper, a partial V_{cm} based switching technique was implemented that requires a digital overhead from the adaptive SAR controller and achieved better conversion accuracy. This methodology has reduced the common mode variation by 50%. Reduction of noise, comparator offset and input parasitic was analyzed and verified by simulation. But, the usage of the external common mode voltage during DAC reset could be a problem with this technique. Large switching power and more area is required to run the entire architecture.

Zhang [8] presented a 14-bit kS/s SAR-ADC used for biomedical application. In order to achieve enhanced linearity, a uniform geometry non-binary weighted capacitive DAC was implemented. Furthermore, in this method, a secondary bit method was used in dynamically shift decision levels for error correction. This method was implemented in 65nm CMOS technology. The ADC has consumed 1.98 µW Power and 0.28mm^2 of active area. This Architecture requires number of stages to implement that increases complexity of the ADC.

Shakibaee [5] proposed a power-efficient adaptive SARADC system. In this design a new low energy capacitor switch approach is used that consumed no switching energy in first three comparison steps. Furthermore, an energy efficient split monotonic method was used for the rest of the operation. In this design switching energy consumption is reduced by 99.23% and total capacitor size is reduced by 75%. The proposed scheme reduced the power consumption of the control logic circuit. The proposed architecture is not suitable for high-resolution ADC circuits.

Some of the properties of adaptive SARADC are:

- Power and area-efficient architecture – the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage
- Only one comparator, two DACs and adaptive SAR logic needed – fits well to modern digital CMOS

The design of adaptive saradc implementation issues are:

III. PROPOSED SYSTEM

In this paper, adaptive SARDAC-ADC circuit is designed which is shown in Figure (1). This architecture contains a DAC,

Analog input, Amplifier, SAR, Sample and hold, Timing circuitry, Adaptive SAR, Comparator and an Encoder. For high sampling linearity, bootstrapped switches are used. In this work, different values of the capacitor are used to design the DAC.

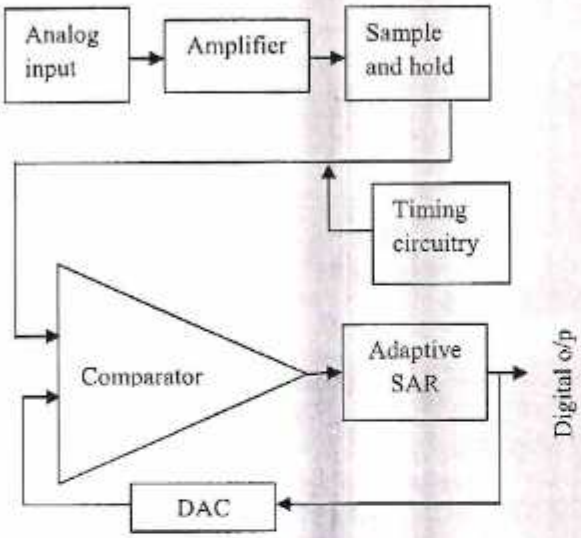

Fig. 1: OVERALL ARCHITECTURE FOR ADAPTIVE SARDAC- ADC CIRCUIT

An amplifier is an electronic circuit used to boost up the strength of the weak signal. This signal can be a current, voltage or power signal. It is a 2 port circuit that increases the amplitude of the input signal and provides an amplified signal at the output end.

Low noise, low power with high speed comparator is an important factor to design the entire architecture.

Figure (2) shows a chain of registers that are cascaded to implement the SAR. The dynamic register is needed to store the comparator outputs and to control the capacitive DAC, D-flip-flops are utilized to accomplish this objective, bringing the critical path delay to 2tdq. tdq is the delay from the rising edge of the clock to the substantial output of a D Flip Flop. In this Architecture, dynamic registers are used, which is activated by the comparator output.

After Ci and C_K goes to low, Ci' is activated to empower the following bit register. Note that Low-Threshold Voltage (LVT) gadgets are processed to further increase the speed.

Fig. 2: ADAPTIVE SARLOGIC DIAGRAM

In electronics, a sample and hold (also known as sample and follow) circuit is an analog device that samples (captures, takes) the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimum period of time. Sample and hold circuits and related peak detectors are the elementary analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.

In electronics, a digital-to-analog converter (DAC, D/A, D2A, or D-to-A) is a system that converts a digital signal into an analog signal. An analog –to –digital converter (ADC) performs the reverse function.

A successive-approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

In timing circuits you are controlling the rate of response of the capacitor or controlling the rate of the voltage across the capacitor. The simplest timing circuit is a series combination of a resistor and capacitor. The time constant is the amount of time to charge the capacitor to 63% of the input voltage and is equal to the resistance times the capacitance (T = RC).

IV. RESULTS

This proposed architecture was implemented initially, each and every sub blocks are designed which helps to create the entire architecture cell view. For making cell view, initially the circuit design needs to be designed. Once it is finished, we have to choose "create ⟶ cell view ⟶ from cell view".

This above step is used to convert schematic into the cell view block. Then, all the cell view is connected to make a main module block design. After the top module design, following performance has been evaluated.

A. Area

The entire area of the architecture is calculated with the help of the transistor. Based on the number of transistors for every block, the area has been calculated.

B. Power and Current

After, running the simulation the power and current consumption of the entire architecture has been calculated. In Analog Design Environment (ADE) window, we have to calculate the power for the top module. For that have to select "Results ⟶ Print ⟶ transient operating point".

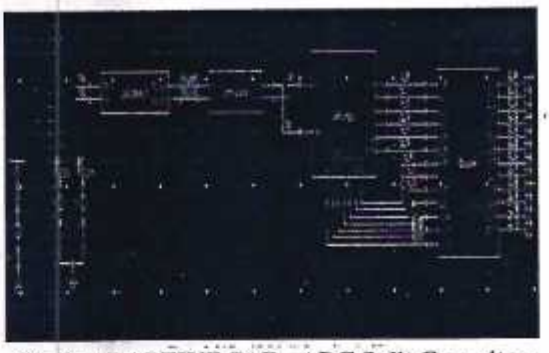

Fig. 3: ADAPTIVE SAR– ADC Split Capacitor Architecture

Figure 3 shows the overall architecture it consists of DAC, comparator, adaptive SAR logic, and encoder. To design 12 bit DAC 48 MUX is required and each MUX needs 2 transistors, one PMOS and one NMOS is enough to design the MUX. The selection line signal is given to the gate terminal.

Fig. 4: OUTPUT WAVEFORM

The comparator operation and schematic is described in the previous section. The adaptive SAR logic explanation and internal block of CU also explained in the previous section.

V.CONCLUSION

The presentation of detailed analysis with the parasitic effects in different switched capacitor DAC topologies as well as their analyzed influence on the minimum value of the unit capacitance and on the total area of the total capacitive array that is shown in this paper. It is shown that even though the spilt capacitor topologies have the main contribution in decreasing the capacitive array area, with the performance as well as

linearity preservation will not be always followed by the area savings. It is shown that the results of 12-bit resolution while using the minimum capacitor available in our 180 nm CMOS technology is almost the limiting resolution for SAR ADCs along with the switched capacitor DAC without the compensation or calibration circuits in this technology.

VI. REFERENCES

[1] Sein Oh ; Younggyun Oh ; Juyoung Lee ; Kihyun Kim ; Seungjun Lee ; Jintae Kim ; Hyungil Chae, "A 80dB DR 6MHz Bandwidth Pipelined Noise-Shaping adaptive SAR ADC with 1–2 MASH structure" 2020 IEEE CONFERENCE PAPER.

[2] Yuichiro Kobayashi, Tatsuji Matsuura, Ryo Kishida, Akira Hyogo, "Investigation of Hybrid ADC Combined with First-order Feed forward Incremental and SARADC" 2019 ISPACS IEEE.

[3] Qingjun Fan, Jinghong Chen "A 500-MS/s 13-Bit SAR-Assisted Time-Interleaved Digital - Slope ADC", 2019 IEEE conference ISCAS.

[4] Uma Mukund Kulkarni ; Chetan Parikh ; Subhajit Sen, "A Systematic Approach to Determining the Weights of the Capacitors in the DAC of a Non-binary Redundant SARADCs" 2018 IEEE.

[5] Shakibaee, Fatemeh, Fereshteh Sajedi, and MEHDI SABERI. "Low-Power successive approximation ADC using split -monotonic capacitive DAC." IET circuits, devices & systems 12.2 (2017): 203-208.

[6] Xing, dezhi, yan zhu, chi-hang Chan, sai-weng sin, fan ye, junyan ren, u. Seng-pan, and rui Paulo martins. "Seven-bit 700-ms/s four-way time-interleaved SAR ADC with partial V_{cm} based switching." IEEE transactions on very large scale integration (VLSI) systems 25, no. 3 (2017): 1168-1172

[7] Wan Kim ; Hyeok-Ki Hong ; Yi-Ju Roh ; Hyun-Wook Kang ; Sun-Il Hwang, Dong-ShinJo, Dong-Jin Chang, Min-Jae Seo, Seung-Tak Ryu. "A 0.6 V 12 b 10 MS/s Low-Noise Asynchronous SAR-Assisted Time - Interleaved SAR (SATI- SAR) ADC" IEEE Journal of Solid-State Circuits, 2016.

[8] Zhang, Dai, and Atila Alvandpour. "A 12.5-ENOB 10-KS/S redundant SAR ADC in 65-NM CMOS." IEEE transactions on circuits and systems II: express briefs 63, NO. 3 (2016): 244-248.

[9] S. Roshany ; M. B. Ghaznavi-Ghoushchi, "A new low power profile for mixed-signal design of SARADC in Wireless Sensor Network applications" 2011 19th Iranian Conference on Electrical Engineering.

[10] He Yong ; Wu Wuchen ; Meng Hao ; Zhou Zhonghua, "A 14-bit successive-approximation AD converter with digital calibration algorithm" 2009, Conference Paper, IEEE.

[1]P VENKATESWARARAO he is working as Assistant professor in the Department of Electronics and Communication Engineering at VIKAS College of Engineering and Technology, Vijayawada rural, Andhra Pradesh, India

[2]SEKHAR VEMPATI is working as Assistant professor in the Department of Electronics and Communication Engineering at VIKAS Group of Institutions, Vijayawada rural, Andhra Pradesh, India.

[3]SARNALA BUTCHI BABU, working as Assistant Professor in the Department of Electronics and Communication Engineering at VIKAS College of Engineering and Technology, Vijayawada rural,

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